UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/716,791	11/19/2003	Hiroaki Kubo	JP920020167US1	6146

7590 04/14/2009

DOUGLAS W. CAMERON
Intellectual Property Law Dept.
IBM Corporation
P.O. Box 218
Yorktown Heights, NY 10598

EXAMINER	
WERNER, DAVID N	
ART UNIT	PAPER NUMBER
2621	

MAIL DATE	DELIVERY MODE
04/14/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/716,791
Filing Date: November 19, 2003
Appellant(s): KUBO ET AL.

Anne Vachon Dougherty
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief 14 January 2009 appealing from the Office action mailed 09 July 2008.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is substantially correct. The changes are as follows: The third document over which claims 1–7 are rejected is U.S. Patent 5,671,260, not U.S. Patent 5,983,237 as given in the Appeal Brief.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,233,253	SETTLE ET AL.	5-2001
6,297,794	TSUBOUCHI ET AL.	10-2001
5,671,260	YAMAUCHI ET AL.	09-1997

ISO/IEC International Standard 13818-1:2000(E) (Dec. 1, 2000), pp. xi-xiii, 18-30, 125.

Chernock, R.S. et al., _Data Broadcasting_ (April 16, 2001), pp. 44-51.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 6,233,253 B1 (Settle et al.) in view of US Patent 6,297,794 B1 (Tsubouchi et al.), of which corresponding Japanese Patent Application Publication 10-116,064 A was cited in the Information Disclosure Statement of 01 March 2007, and in view of US Patent 5,671,260 A (Yamauchi et al.). Claims 1, 6, and 7 of the present invention are co-extensive in scope with claim 1 as a hardware embodiment, claim 6 as a method, and claim 7 as a software embodiment. Settle et al. teaches a format conversion system that multiplexes video data from multiple sources into one data format for

transmission (abstract). Regarding the “header generation device” of apparatus claim 1, packetizers 18 in Settle et al. add MPEG transport headers to the data from the video sources (column 4: lines 47-49). Regarding the step of “generating a packet header” in method claim 6, the packetizers perform formatting steps 214 and 245, which add packet headers to video data in the method shown in figure 1 of Settle et al. (column 3: lines 23-29, 50-52). Regarding the step of “generating the packet header” in software claim 7, the packetizing method may be implemented on a computer (column 4: lines 26-30). Regarding the "selection of a predetermined amount of video data of said memory as a payload responsive to the packet header" in claims 1, 6, and 7, Settle et al. produces MPEG-2 transport stream packets (column 4: lines 39-42), which were known to have a fixed length of 188 bytes each, comprising the packet header and packet payload data.

Although in the header-generating device of Settle et al. clock references are periodically added to a resultant multiplexed transport stream (column 5: lines 63-66), this information is used to synchronize audio and video data at a decoding step, not at encoding, and so does not correspond with the claimed "synchronizing signal”.

Tsubouchi et al. teaches a system with a variety of video devices, including a video capture device (column 8: lines 17-25) and MPEG encoder (column 6: lines 50-58), which share a dedicated bus for audio/video data. Each device includes an output buffer for outputting data onto the bus (column 2: lines 55-57). This bus includes a ZV control line, on which an enable signal can be transmitted. The control line may be daisy-chained to each device (column 5: lines 27-36), or it may be common to all

devices (column 10: lines 13-15). In one embodiment, a pulse generating circuit in each device sends out a pulse on the control line to disable other devices and free up the A/V bus for data transmission (column 11: lines 32-58). Then, the enable signal corresponds with the claimed "synchronizing signal". The setup is pulse-width modulated, with each pulse generating circuit producing a pulse of a different width (column 11: lines 10-32). Each device also includes a flip-flop that stores the enable/disable state for the device. A particular device can only use the video when its flip-flop is set to enable (column 10: lines 41-56). Then, until a pulse from a different device is detected, resetting the flip-flop, a device may be free to output video to the bus. Then, these flip-flops correspond with the claimed “synchronous timing detector” in claim 1, and the resetting of a flip-flop corresponds with the claimed “detecting a synchronization signal”.

Settle et al. discloses a majority of the claimed invention except for generating packetized video in response to a synchronization signal. Tsubouchi et al. teaches that it was known to store video in a buffer, and only read out from the buffer in response to an enable signal. Therefore, it would have been obvious at the time the invention was made to store video from a source into a buffer and only output from the buffer after detecting an enable signal, as taught by Tsubouchi et al., since Tsubouchi et al. states in column 2: lines 49-50 that such a modification would prevent collision between video data streams from multiple sources.

However, the combination of Settle et al. alone and Tsubouchi et al. the enable pulse in Tsubouchi et al. for reading video data from the buffer is not a horizontal

synchronization signal, operating on digitized video data comprising a plurality of data lines, each followed by a horizontal synchronization period.

Yamauchi et al. teaches a digital signal processing apparatus that includes a Phase Locked Loop (PLL) that produces a clock signal locked to the horizontal synchronization signal included with the video input (abstract). Regarding claims 1, 6, and 7, Synchronization signal 2 extracts an HSYNC and VSYNC signal from input video signal Sv (column 4: lines 44-50), and control generator 12 extracts the HSYNC signal to produce reference signal Sf1 (column 2: lines 51-56). PLL 13 generates a clock signal Sc1 from reference signal Sf1 (column 4: lines 61-63), and A/D converter 5 samples video signal Sv with respect to the clock signal Sc1, producing digital video Svc (column 5: lines 27-32), comprising lines of digital video synchronized to horizontal and vertical synchronization signals (column 8: lines 1-49). (Compression of the digital video, commonly known to include the steps of converting from a video line format to a transform format of two-dimensional blocks of data, does not occur at this stage.) Digital video Svc is stored into memory 6 based on write signal Sw, which is based on the HSYNC and VSYNC signals from the original video (column 5: lines 24-26). Then, the video memory is only written to when video data is transmitted in signal Sv, such as columns 123–824 in a given line in the NTSC standard (column 5: lines 19-24).

Settle et al., in combination with Tsubouchi et al., disclose the claimed invention except for digitizing video according to a horizontal synchronization signal. Yamauchi et al. teaches that it was known to sample video based on a horizontal synchronization signal, as set forth in column 5: lines 6-39. Therefore it would have been obvious to one

having ordinary skill in the art at the time the invention was made to synchronize a digital video transcoder to HSYNC as taught by Yamauchi et al., since Yamauchi et al. states in column 8: lines 1-4 that such a modification would ensure that only relevant video data is encoded and not non-video data transmitted in a horizontal blanking interval, regardless of the variability of this interval.

Regarding claim 2, as mentioned previously, Settle et al. produces MPEG-2 transport stream packets (column 4: lines 39-42). As was known in the art at the time of the invention, an MPEG-2 transport stream packet must be 188 bytes long, and consists of a header and a payload. If the header is given an extended length, then the subsequent payload is shortened so that the total length of the header and the payload remains at 188 bytes. As shown in ISO/IEC 1318-1 (MPEG-2), a transport stream includes an "adaptation field length" field that indicates the length, in bytes, of the extended header (pp. 21). Therefore, since Settle et al. is an MPEG-2 transport stream encoder, it is inherent that it includes counters for counting packet header length and total packet length, and a selector to output payload data after a packet header has concluded, to produce valid MPEG-2 transport stream packets.

Regarding claim 3, as discussed at length above, Settle et al. outputs video data as MPEG-2 transport stream packets. In addition, video capture 31 of Tsubouchi et al. contains an output buffer for outputting video to a dedicated bus (column 2: lines 55-57), corresponding with the FIFO memory.

Regarding the "data valid signal" of claim 4, in Yamauchi et al., video memory write signal Sw is only enabled during the period in a particular line in a video when converted video signal Svc corresponds to effective video data (column 5: lines 17-26). Then, only valid video data is transmitted.

Regarding the memory reset in claim 5, for each given line in an NTSC format, writing signal Sw controls a memory to not read data for the first 122 cycles of clock Sc1 produced from the horizontal synchronization signal, then to write data for the next 720 clock cycles, and to release data, thus clearing and resetting the memory for the next line, for the last 16 clock cycles (column 8: lines 1-15).

Yamauchi discloses the claimed invention except for producing a data valid signal based on a horizontal synchronization signal from a memory write controller instead of a packet header length counter. However, the "data valid signal" in claims 4 and 5 is considered equivalent under the Doctrine of Equivalents to the "writing signal" in Yamauchi et al., since in both the present invention and in Yamauchi et al., the signal performs the same function (controlling a memory storing a video signal), in substantially the same way (in response to a horizontal synchronization signal), to produce substantially the same result (outputting only valid data not in the horizontal blanking interval). See *Graver Tank & Mfg. Co. v. Linde Air Products*, 339 U.S. 605, 85 USPQ 328 (1950).

(10) Response to Argument

Appellant's arguments regarding claims 1–7 have been fully considered but are unpersuasive.

Claims 1, 6, and 7

35 USC 103(a) as unpatentable over Settle in view of Tsubouchi and Yamauchi

Considering independent claims 1, 6, and 7, Appellant states that the cited references, in combination, do not disclose every limitation of the present invention. Three specific alleged faults are mentioned: first, the alleged failure of the Settle reference to produce packets including a "packet header" and "a predetermined amount of video data", second, the alleged failure of the Tsubouchi et al. to disclose the claimed "synchronous timing detector" or "synchronous timing detecting device", and third, the alleged failure of Yamauchi et al. to disclose the claimed "synchronizing signal for a line of video data", in which the line of data includes a "horizontal synchronizing period". Appellant's arguments based on remaining claims 2–5 either are reiterations of, or depend on, these three main arguments.

First, regarding Settle, Appellant states that "MPEG compatible packets" produced by Settle are not necessarily packets having "a fixed packet length" (pg. 10), which the Examiner interprets the meaning of the claimed "predetermined amount of

video data" selected "as a payload responsive to the packet header", and particularly cites column 4: line 49 which states that "MPEG compatible packets" are formed. However, the reference elsewhere explicitly states that these packets are MPEG transport packets, which inherently have a fixed length. See for example, column 3: lines 24–25, "MPEG compatible transport packet form"; column 4: line 8, "MPEG compatible transport datastream"; and column 4: line 40, "MPEG transport packets". Considering this, it is respectfully submitted that Settle produces the claimed packets.

Next, regarding Tsubouchi et al., applicant states that the data bus cited in the Final rejection as delivering the claimed "synchronizing signal" does not necessarily operate on "digitized" data as required in the preamble of claim 1, and so is not applicable to the present invention (pp. 11–12). However, it is respectfully submitted that in the figure 1 embodiment, the data bus 4 may receive as input data from video capture 31, which performs steps of "Converting analog video signals from an imaging device such as a video camera to digital data, and inputting the digital data" (column 1: lines 45–47). The bus may also be connected to other digital devices such as an MPEG-2 decoder or an IEEE 1394 controller. Considering this, it is respectfully submitted that Tsubouchi et al. operates on digital data.

Lastly, regarding Yamauchi et al., Appellant states that Yamauchi describes a system in which a reading operation from a data buffer is controlled exclusively with a signal based on a vertical synchronization period of a video, and so is not applicable to the claimed invention, in which data is read from a memory responsive to a horizontal synchronization of the video (pp. 13–14). Appellant does not consider the write signal,

described in the Yamauchi et al. reference as controlled by the horizontal synchronization period, to be relevant (pg. 14). However, it is respectfully submitted that this improperly characterizes the combination of the Tsubouchi et al. and Yamauchi et al. references. The combination was not a matter of simple substitution, in which the read signal of Tsubouchi et al. was replaced by the read signal of Yamauchi et al., but rather, Yamauchi et al. was cited to demonstrate that it was known in the art to use the horizontal synchronization of a raster video signal to perform control operations of a buffer, with the result of not digitizing or transmitting non-video data presented during the horizontal control period. The standard for obviousness over a combination of references is not whether the structural features of the references are physically combined. Instead, a combination of the **teachings** of the references is required. *In re Keller*, 642 F.2d 413, 425, 208 USPQ 871, 881 (CCPA 1981); *In re Nievelt*, 482 F.2d 965, 179 USPQ 224, 226 (CCPA 1973).

Claim 2

Regarding claim 2, the examiner re-iterates that the "MPEG compatible" packets of Settle are explicitly described as in the fixed-length "transport packet form" in a "transport stream", and must inherently have 188 bytes. Any encoder or processor that produces data in the MPEG "transport packet form" must inherently include the claimed counter and switch to output valid packets. See also Chernock, R.S. et al., *Data Broadcasting*, pp. 44–51, which describes the MPEG-2 transport stream syntax.

Claim 3

Regarding claim 3, the examiner again re-iterates that the "MPEG compatible" packets of Settle are explicitly described as in the fixed-length "transport packet form" in a "transport stream", and so these packets, containing data other than MPEG-format video as payload (column 3: lines 1–5) are the claimed "pseudo MPEG2-TS" packets. Additionally, in Yamauchi et al., a horizontal synchronization signal or a vertical synchronization signal, or their derived "clock" signals sc1 and sc2 which drive the controllers of a memory, may be the claimed "clock" that drives the FIFO.

Claim 4

Regarding claim 4, the examiner re-iterates that the combination of Tsubouchi et al. and Yamauchi et al. is not to bodily incorporate the read signal determined from a vertical synchronization of Yamauchi et al. into the buffer of Tsubouchi, but merely that it was known in the art to control the timing of a buffer operation based on horizontal synchronization, as in the write signal of Yamauchi et al.

Claim 5

Regarding claim 4, the examiner again re-iterates that the combination of Tsubouchi et al. and Yamauchi et al. is not to bodily incorporate the read signal determined from a vertical synchronization of Yamauchi et al. into the buffer of Tsubouchi, but merely that it was known in the art to control the timing of a buffer operation based on horizontal synchronization, as in the write signal of Yamauchi et al.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/D. N. W./

Examiner, Art Unit 2621

Conferees:

/Mehrdad Dastouri/

Supervisory Patent Examiner, Art Unit 2621

/Thai Tran/

Supervisory Patent Examiner, Art Unit 2621